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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,443	01/06/2004	Hongmei Wang	M4065.0536/P536-B	2565

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EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,443	WANG ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27 and 32-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27 and 32-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/05,3/21/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: M4065.0536/P536-B

Filing Date: 1/6/2004

Claimed Priority Dates: 11/26/2002 (Continuation of 10/303,696)
6/5/2002 (Divisional of 10/161,615)

Applicant(s): Wang, et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 3/21/2005.

Acknowledgment

1. The amendment filed on 5/19/2005, responding to the Office action mailed on 3/21/2005, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 27 and 32-35.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description (see, *e.g.*, par.0041/II.6) with respect to figure 19: **100**.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the gate stack including a p-type conductive layer in a partially depleted SOI NMOS transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

4. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended

replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 27 and 32-35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

7. Lines 9-10 of claim 27 recite a gate stack for a fully depleted (FD) SOI NMOS transistor including a p-type conductive layer. Lines 14-15 of claim 27 recite a gate stack for a partially depleted (PD) SOI NMOS including a p-type conductive layer. The description in the original disclosure fails to support these limitations in the claim. Although the specification shows a p-type conductive layer for the FD transistor, it differently shows an n-type conductive layer for the PD transistor (see, *e.g.*, par.86/ll.8-9 and figs. 19-20).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

10. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 27 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US 6484065) in view of Houston (US 6424016).

12. Regarding claim 27, Yu (see, *e.g.*, fig. 1) shows most aspects of the instant invention including a processor-based system **100** comprising

- A processor **110**
- An integrated circuit **120** coupled to the processor **110**

wherein the circuit comprises a transistor, the transistor comprising source/drain regions of a first conductivity type and a gate stack including a conductive layer.

Although not explicit, Yu shows the circuit including DRAM banks **120a-d**, which by definition are made of transistors, each with its respective first-conductivity-type source/drain regions and conductive-layer gate stack.

Yu, however, fails to specify that the source/drain regions and the gate stack be provided on an SOI substrate and that the conductive layer of the gate stack is of a second conductivity type.

Houston (see, *e.g.*, col.1/ll.14-25), on the other hand, teaches that SOI substrates are good for DRAMs for several reasons. One reason is that SOIs have lower collection volumes.

Like Yu, Houston (see, *e.g.*, figs. 5-6 and col.4/ll.54-58) also shows DRAMs including transistors having source/drain regions of a first conductivity type (n-type) and a gate stack **40** including a conductive layer of a second conductivity type (p-type). These are fully depleted SOI NMOS **40 41** forming part of a memory array (see, *e.g.*, col.5/ll.52-53).

Houston also shows a partially depleted SOI NMOS transistor **42** comprising source/drain regions provided on the substrate. The source/drain regions are of n-type

conductivity (see, *e.g.*, col.5/ll.54-56 and col.6/ll.7-9). A second gate stack is fabricated on the substrate including a conductive layer of a p-type conductivity (see, *e.g.*, col.5/ll.50-51).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Yu's integrated circuit comprising fully-depleted and partially-depleted transistors having gate stacks and source/drain regions provided on an SOI substrate, wherein the gate stacks are p-type and the source/drain regions are n-type, as suggested by Houston, to lower the collection volume of the integrated circuit.

13. Regarding claim 32, Houston shows that the conductive layer of the gate stack is a doped polysilicon layer (see, *e.g.*, col.5/ll.50).

14. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu/Houston in view of Krivokapic (US 6452229).

15. Regarding claim 33, Yu/Houston shows most aspects of the instant invention (see, *e.g.*, paragraphs 11 and 12 above), except for the conductive layer being doped silicon/germanium.

Krivokapic, on the other hand, teaches (see, *e.g.*, col.4/ll.1-7) that doped silicon/germanium is an equivalent gate material to the doped polysilicon of Yu/Houston.

Therefore, because these two gate materials were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute Yu/Houston's doped polysilicon for the doped silicon/germanium that Krivokapic suggested.

16. Claims 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu/Houston in view of Wu (US 6060749).

17. Regarding claims 34 and 35, Yu/Houston shows most aspects of the instant invention (see, *e.g.*, paragraphs 11 and 12 above), except for at least one of the gate stacks further comprising a silicide layer or a cap layer over the conductive layer.

Wu (see, *e.g.*, col.5/ll.9-18), on the other hand, teaches that having a silicide cap layer over Yu/Houston's polysilicon gate will reduce the parasitic resistance of the gate.

It would have been obvious at the time of the invention to one of ordinary skill in the art to form a silicide cap layer over Yu/Houston's polysilicon layer, as suggested by Wu, to reduce the parasitic resistance of the gate.

Response to Arguments

18. The applicants argue:

> Yu does not show an SOI substrate with FD and PD transistors formed in memory and array areas, respectively, as recited in claim 27. Houston, on the other hand, does not show an integrated circuit coupled to a processor, as also recited in claim 27.

The examiner responds:

One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Yu and Houston were combined to render obvious the limitations in claim 27 (see, *e.g.*, paragraph 11 above).

19. The applicants argue:

> Houston fails to show an FD NMOS transistor comprising n-type source/drain regions and a p-type gate in a memory array, nor does he show a PD transistor comprising n-type source/drain regions and a p-type gate in a peripheral region. Houston differently shows an n-type gate for an FD pass transistor and a p-type gate for a PD periphery transistor (see, *e.g.*, col.6/ll.15-24).

The examiner responds:

Houston clearly shows an FD NMOS transistor **41** in a memory region (see, *e.g.*, fig. 5) comprising n-type source/drain regions and a p-type gate (see, *e.g.*, col.4/ll.55-57 and col.5/ll.51-53). He also shows a PD transistor **42** in an array region (see, *e.g.*, fig. 5) comprising n-type source/drain regions and a p-type gate (see, *e.g.*, col.5/ll.51,54-56 and col.6/ll.7-9).

Conclusion

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

21. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center

number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

24. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

25. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/347-354,407	6/2/2005
Other Documentation: PLUS Analysis	3/15/2005
Electronic Database(s): EAST (USPAT, EPO, JPO)	6/2/2005

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